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A NETWORK MODELING AND DESIGN METHOD FOR A 2-18 GHz FEEDBACK AMPLIFIER

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ABSTRACT

An accurate network theory and modeling method, including feedback loop circuit parasitics and device limitations, is presented for the design of broadband microwave feedback amplifiers. Discussed are circuit realization and measured performance in relation to VSWR, gain flatness and stability of a 2 to 18 GHz three stage amplifier.

INTRODUCTION

The application of controlled feedback to improve the performance of solid-state and vacuum tube amplifiers is well known. However, as the upper frequency demands on wideband MESFET amplifiers increase, accurate feedback design using classical techniques, which employ ideal elements (R, L, C), becomes exceedingly difficult. The effects of FET mounting, bond wire lengths and element parasitics, if not included in the design approach, degrade the validity of the resulting computed amplifier performance.

In this work a method to design multi-stage single-ended feedback amplifiers with extended high frequency performance is outlined. Included in this outline are the design, analysis and measured performance of several amplifiers as well as the application of this modeling method to monolithic circuit design. Although the user requires some form of computer aided circuit analysis capability, due to the complex circuit modeling, he can quickly and easily analyze/optimize the desired amplifier using one of the Microwave CAD Programs currently available.

AMPLIFIER DESIGN TECHNIQUES

One of the prime areas of difficulty in designing cascaded MESFET amplifiers is controlling the impedance match between devices.[1] Shunt feedback can be used to reduce the magnitude of S_{11} and S_{22} at the terminals of the active elements, thus enabling the circuit designer to synthesize wideband matching networks. Flat gain versus frequency and greatly improved amplifier stability, especially at lower microwave frequencies, are also desirable byproducts of feedback.[2,3] This improved circuit performance is not without cost; it is obtained at the expense of reduced transducer gain.

The simplified single stage smplifier model shown in Figure 1 can be analyzed using computer aided design methods to determine the approximate amount of RF feedback that will produce the best compromise of the above performance parameters. The effects of increasing shunt RF feedback on a typical FET is shown in Figure 2. As the amount of feedback is increased (lower values of R_F) the magnitude of S_{11} and S_{22} are greatly reduced; however, this process cannot continue indefinitely since the maximum available gain of the device becomes too low to be of practical use. Even though S_{11} and S_{22} are not reduced to zero, the required transformation ratio of the matching networks is small enough to allow for the easy design and realization of input/output and interstage networks.

As the operating frequency of the amplifier is increased, only small amounts of negative feedback can be tolerated, since the open loop gain of the active device is becoming marginal. The natural gain rolloff of the FET is then compensated by reducing the amount of negative feedback at the upper frequency portion of the operating band. Typical values of S_{11}, S_{22} and G_{MAX} are also shown in Figure 2.

Based on the above analysis, a feedback loop is synthesized using ideal elements (R, L, C) and the resulting gain stage demonstrates a computed frequency response extending to 18 GHz. However, when the appropriate circuit parasitics, which are always present with any practical circuit realization, are included, the high frequency performance of the amplifier is diminished. A circuit model for the true feedback loop including phase length and parasitics of the thin film resistors, bond wire characteristics, distributed inductance and capacitance effects will now be discussed.

At frequencies above 14 GHz, the amplifier performance degradation due to these effects are pronounced. The active device mounting parasitics and phase transfer characteristics also greatly influence final circuit performance. To begin the model formulation the FET must be characterized with the same mounting parasitics that will be present in the final amplifier. Thus, if self biased amplifier operation is desired, S-parameter characterization should be performed with the correct values of source lead inductance and RF by-pass capacitors. The input/output bond wire lengths which were used when the FET was mounted in the test fixture, should be maintained in the final amplifier circuit. A FET with high reverse isolation, low transducer phase shift and a large transducer gain is essential in obtaining extended Ku band performance. The total loop and transducer phase shift must be maintained such that large amounts of positive feedback do not occur. Although small amounts of positive feedback can improve the high frequency gain performance, large amounts of feedback can cause gain instability as a function of temperature as well as oscillation.

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In order to minimize the phase shift encountered in the feedback loop the resistor is deposited on the substrate using conventional thin film methods and the surface area is kept as small as manufacturing constraints will permit. Although the feedback resistor is usually less than .005 x .010 inch, its frequency response characteristics can be modeled as a ladder network consisting of several resistor/transmission line sections. The network commonly used consists of 6 sections, where $R_F = R_{FTOT}/N$ and $T_{F1} = (Z_R, \theta_S/N)$. The value of Z_R is the equivalent microstrip impedance corresponding to the feedback resistor width. The feedback inductance and resistor end pads are modeled as lossless transmission lines. A series/shunt model for the DC blocking capacitor includes its mounting effects. Constrained computer aided optimization techniques restored the high frequency performance of the circuit shown.[4] The appropriate input/output or interstage network model can now be added to complete the amplifier design. The resulting single state feedback amplifier model is shown in Figure 3.

MEASURED PERFORMANCE

A variety of multi-stage amplifiers, constructed on various substrate materials have been designed. The 2 to 10 GHz two stage amplifier shown in Figure 4 was assembled on a .020 inch thick fused silica substrate. Nichrome thin film resistors are used in the bias circuits and feedback network, and the required series inductance was realized with inductors wound with .001 inch diameter gold wire. Figure 5 depicts the two stage amplifier's measured input/output VSWR and gain versus frequency response.

Since the input/output VSWR of this amplifier is low, several two stage gain blocks can easily be cascaded without the need for balancing; thus, a reduction in amplifier size and number of devices needed for a particular gain requirement is achieved. The 2 to 18 GHz three stage amplifier and its associated gain versus frequency response are shown in Figures 6 and 7 respectively. A second amplifier which uses different FET's and self biasing, was assembled with the same thin film networks. The gain versus frequency response of the amplifier is shown in Figure 8. Fabrication of this amplifier was accomplished using thin film circuit techniques on .010 inch thick alumina (Al_2O_3) substrates. Key to the amplifier's ability to perform at Ku band frequencies is the minimization of the effective phase length of the feedback loop and its associated parasitics by controlling the separation of the input, interstage, and output substrates and by using ultra small (.010 inch square) DC blocking capacitors.

CONCLUSION

The illustrated design method enables the microwave engineer to easily synthesize and analyze broadband feedback amplifiers with an added degree of confidence that the current simple circuit modeling techniques could not predict. The new circuit model and design philosophy are especially valuable at frequencies above 14 GHz. The excellent stability and impedance control characteristics allow amplifier gain chains to be constructed with cascaded multistage feedback gain blocks, certainly an important factor in reducing the cost, complexity and size over conventional designs employing cascaded balanced hybrid coupled gain stages. Since these feedback techniques are applicable to monolithic circuits, accurate circuit modeling aids in the design of stable, single-ended amplifiers, where costly design iterations and balanced configurations are neither desirable nor possible.

Acknowledgement

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1) E. Ulrich, "The Use of Negative Feedback to Slash Wideband VSWR", Microwaves, October 1978, pp 66-70.

2) K. B. Nicalas, W. T. Wilser, R. B. Gold and W. R. Hitchens, "The Matched Feedback Amplifier: Ultrawideband Microwave Amplification With GaAs MESFET's," IEEE Transaction on Microwave Theory and Techniques, Vol. MTT-28, No. 4, April 1980.

3) _____, "A 350 MHz to 14 GHz MESFET Amplifier Using Feedback," Digest of Technical Papers, international solid-state circuit conference, February 1980, pp. 164-165.

4) COMSAT General Integrated Systems, Inc., "Super Compact User Manual," 1981.

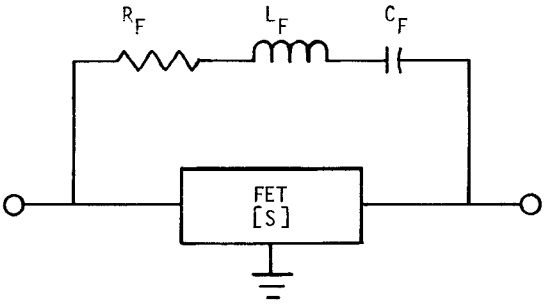


Figure 1. Simplified feedback model.

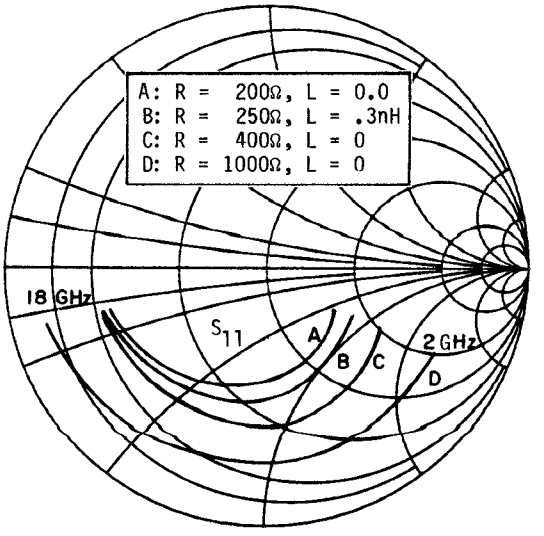


Figure 2a. S_{11} as a function of R_F and L_F.

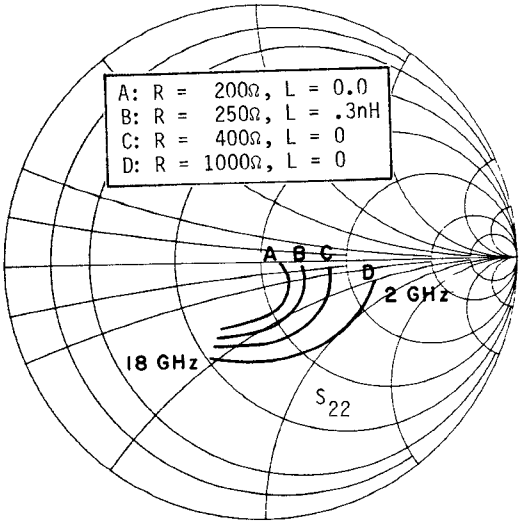


Figure 2b. S_{22} as a function of R_F and L_F.

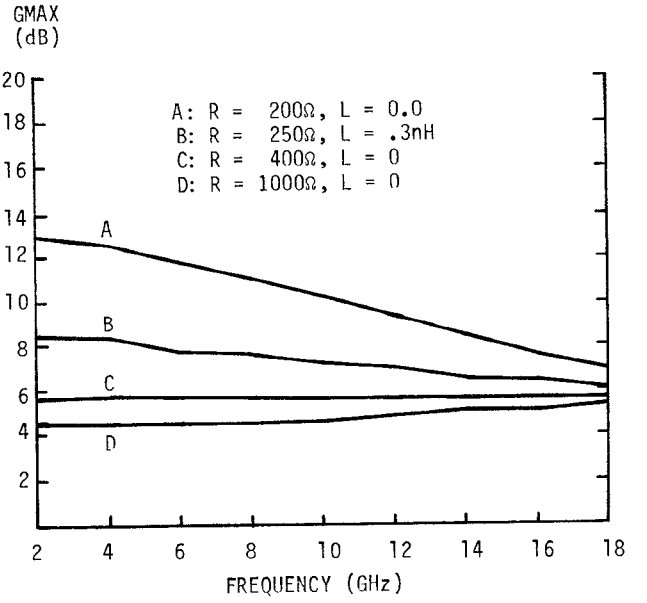
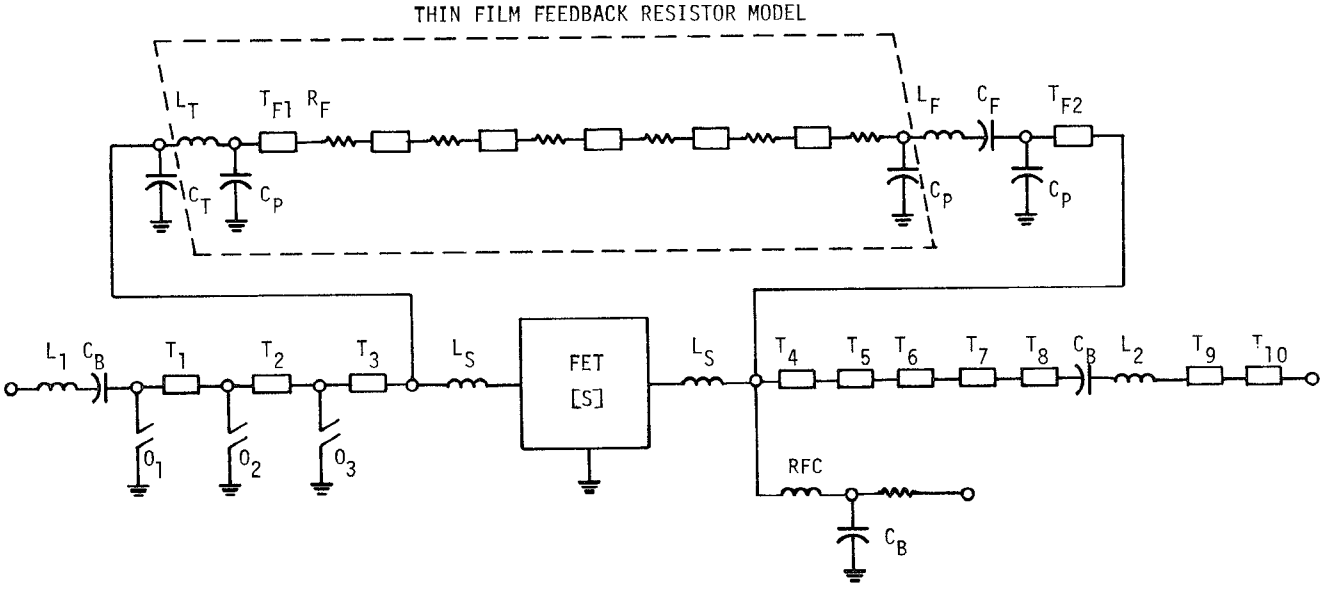


Figure 2c. FET G_{MAX} (dB) as a function of R_F and L_F.



CIRCUIT ELEMENT DESCRIPTION	
C_B	BLOCKING CAPACITOR
C_P	SHUNT PAD CAPACITANCE
C_T	EXCESS "T" JUNCTION CAPACITANCE
L_1, L_2	BLOCKING CAPACITOR MOUNTING INDUCTANCE
L_F	FEEDBACK INDUCTANCE
L_S	EXCESS MOUNTING INDUCTANCE
L_T	EXCESS "T" JUNCTION MODEL INDUCTANCE
O_1 - O_3	OPEN CIRCUIT TRANSMISSION LINE STUB
R_F	INCREMENTAL FEEDBACK RESISTOR
T_1 - T_{10}	SERIES TRANSMISSION LINE FILTER ELEMENTS
T_{F1}	INCREMENTAL TRANSMISSION LINE EQUIVALENT OF R_F
T_{F2}	TRANSMISSION LINE MODEL OF MAIN FEEDBACK INDUCTANCE

Figure 3. Single stage feedback amplifier model.

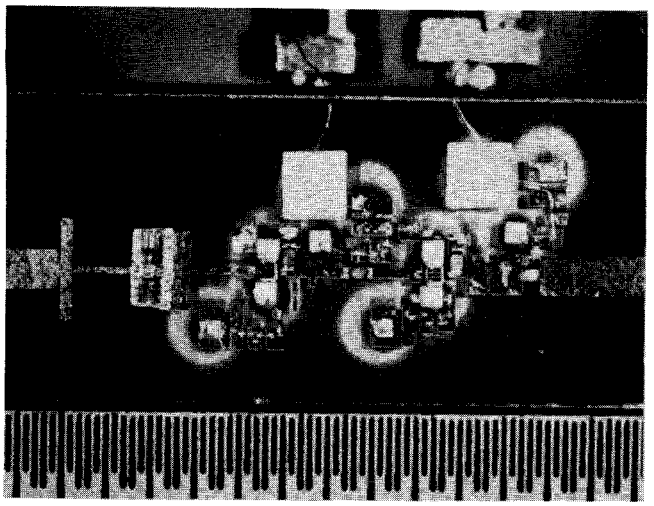


Figure 4. Two stage 2-10 GHz feedback amplifier.

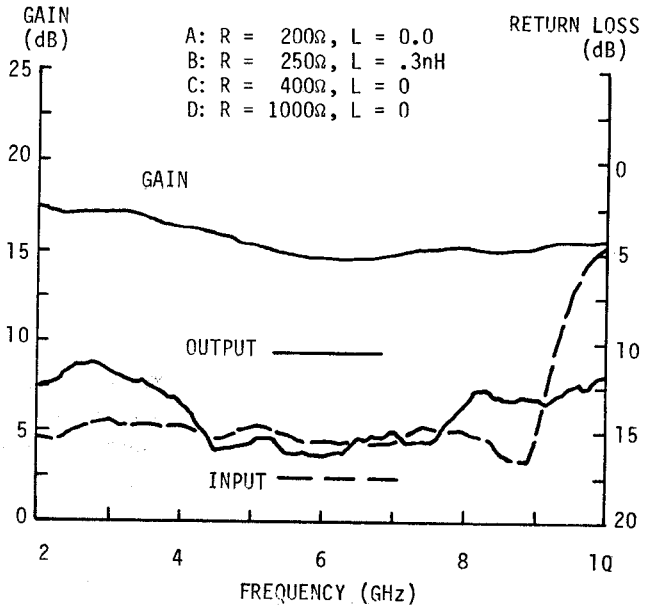


Figure 5. Two stage amplifier performance.

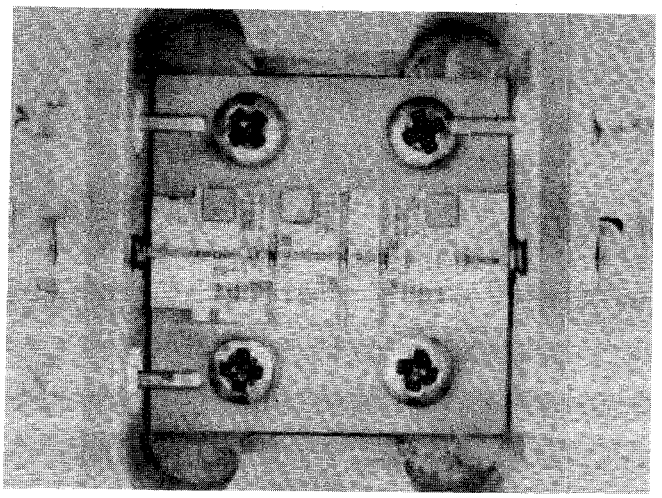


Figure 6. Three stage 2-18 GHz feedback amplifier.

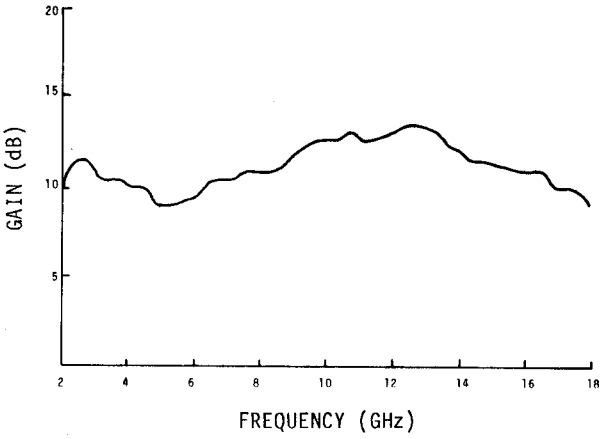


Figure 7. Amplitude response of three stage feedback amplifier.

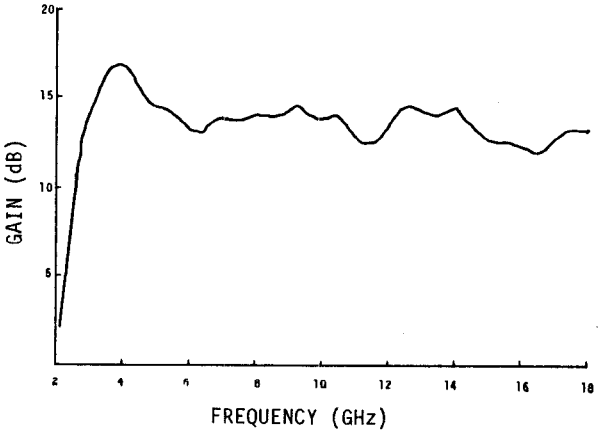


Figure 8. Amplitude response of three stage feedback amplifier.